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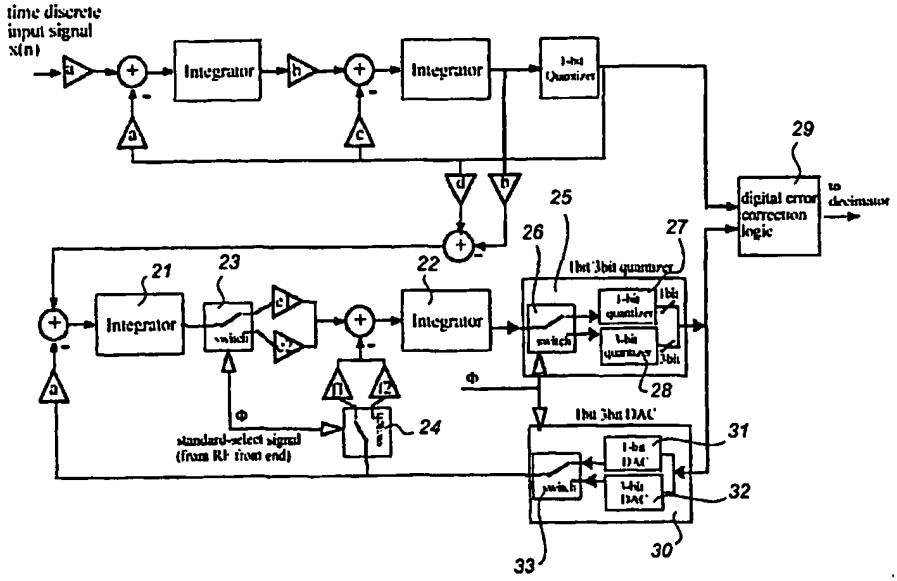

(57) Abstract: The present invention relates to a sigma-delta modulator, which is operative in different standard modes for processing communication signals of different communication standards. The modulator comprises a 1-bit quantizer and a multi-bit quantizer, and a switching mechanism for switching between said quantizers in dependence of the standard mode. The invention further relates to an A/D converter comprising such a modulator, a multi-standard RF receiver comprising such an A/D converter, and a method for signal processing of communication signals of different communication standards.

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A FRONT-END RECEIVER SIGMA-DELTA MODULATOR

Field of the Invention

The present invention relates to sigma delta modulators. More particularly the present invention involves the integration of multi-standard base-band signal A/D conversion for RF receiver into a single sigma-delta modulator.

Background of the Invention

As described in "A 3 V, 2.8 mW CMOS Delta Sigma modulator for GSM applications", Symposium on VLSI Circuits, 1998, P. 90-91, and "A 13-bit, 1.4-MS/s sigma-delta modulator for RF baseband channel applications", IEEE Journal of Solid-State Circuits, Volume 33, Oct. 1998, P. 1462 -1469, sigma delta modulators can be used for GSM and DECT base-band signal A/D conversion. Other wireless standards such as DCS1800, PHS can also use a sigma delta modulator to convert its base-band signal as long as the signal band can be handled by oversampling sigma delta modulators. The base-band width of such standards can range from about 100k Hz to several Mega-Hz. The dynamic range requirement of the A/D converter is determined by the receiver front-end architecture. The reasons of using a sigma delta modulator in such applications are mainly to achieve high resolution, to reduce the strict requirement on analog anti-alias filter, to make the use of cheap and robust CMOS process and to achieve high level integration of the whole RF receiver system.

A multi-standard RF receiver should be able to process multi-standard signal in a single terminal. Accordingly the A/D converter in such a receiver terminal should have the capability to convert the analog signals with different bandwidth and dynamic range requirements.

Since these requirements can vary in a very wide range, the optimization of such an A/D converter is difficult. A straightforward method is to design the A/D converter according to the strictest specification from all the standards. This will, however, increase the chip area and cost, and reduce the integration level. Another solution is to use a unique A/D converter for every standard, with each of these converters optimized for its specific standard. Obviously this solution has the same drawback as mentioned.

Yet another solution is disclosed in EP 0757446, where a sigma delta modulator is provided with an adjustable conversion rate in order to be adaptable to different standards, primarily GSM and DECT respectively.

Summary of the Invention

It is an object of the present invention to provide a structure of multi-standard sigma delta modulator for RF receivers, by means of which structure the power consumption is reduced.

This object is accomplished in accordance with the present invention by sharing most of the modulator hardware for all of the standards, while switching part of the modulator hardware into use for each specific standard. In this way maximum integration is achieved while at the same time the silicon area and power consumption minimized. The modulator order and topology should be selected with the overall consideration of all the standards' specifications. The modulator can be switched to work under different sampling frequencies to meet the dynamic range specifications from different standards.

More particularly, in one aspect of the invention there is provided a sigma-delta modulator, which is operative in different standard modes for processing communication signals of different communication standards. The modulator comprises a 1-bit quantizer and

a multi-bit quantizer, and a switching mechanism for switching between said quantizers in dependence of the standard mode.

Accordingly the invention provides for a mechanism to switch between a 1-bit and a multi-bit quantizer into use for different standard modes. In some of the standard modes a multi-bit quantizer should be used to achieve the resolution specification, while in other modes a simple one-bit quantizer can be used to save power. In each specific mode, its corresponding quantizer is selected and the unused quantizer is shut down to minimize the overall power consumption.

Further, in accordance with the invention there is provided a capacitor sharing and switching mechanism that uses the same capacitor array to form the switched capacitor circuit needed by different standard modes. The choice of capacitor size is decided by the kT/C noise consideration and loop coefficients.

To verify the feasibility of the above mechanisms a prototype chip has been designed and fabricated with 0.35um standard CMOS process. It converts either GSM or DECT base band signal into digital streams, which can then be handled by DSP block.

Brief Description of the Drawings

The objects and advantages of the invention will be understood by the following detailed description in conjunction with drawings in which:

Figure 1 shows the block diagram of a multi-standard receiver structure;

Figure 2 shows a 2-2 cascaded sigma-delta modulator in accordance with an embodiment of the present invention;

Figure 3 shows the switching between 1-bit and multi-bit quantizers in different standard modes; and

Figure 4 shows the capacitor sharing mechanism in switched capacitor integrator.

Description of embodiments

For a better understanding of the invention, the following detailed description refers to the accompanying drawings, wherein preferred exemplary embodiments of the present invention are illustrated and described.

In a multi-standard receiver that adopts base-band A/D conversion, as shown in figure 1, a RF filter passes the band of interest through an RF/IF process block. This RF/IF process block can have e.g. a direct conversion architecture or a wide-band IF with double conversion architecture. Depending on this specific architecture, the succeeding A/D block should meet a corresponding dynamic range requirement which is decided by the out-of-band noise distribution. This dynamic range normally can range from 8~9 bits to as high as 15~16 bits for different wireless standards. To achieve such a wide dynamic range, using a sufficiently high order sigma-delta modulator is a necessity. Figure 2 shows a 2-2 cascaded modulator according to an embodiment of the present invention. A basic 2-2 cascaded modulator was proposed in "Fouth Order Sigma-Delta Modulator Circuit for Digital Audio and ISDN Application", IEE European Circuit theory and Design Conference, 1989, P. 223-227. This previously proposed modulator comprises the first stage and a straight forward structure of the second stage of the inventive modulator. That straight forward structure has no alternative signal paths; for example it has a single B-bit quantizer and no adjustable loop coefficients. The 4th order noise shaping promises sufficient in-band noise attenuation, and the cascade structure promises stability of feedback loop. In an ideal case the dynamic range of such a modulator is:

$$DN \text{ (in bit)} = 4.5*\log_2 M + \log_2(2^B - 1) - offset$$

Here *M* is the oversampling ratio, *B* is the resolution (in bit) of the second stage's quantizer, and *offset* is a value normally around 7 depending on the detailed scaling factor. In real implementations, due to the circuit non-idealities and kT/C noise, this *offset* can be even larger and the achievable dynamic range is further reduced.

In accordance with an embodiment of the modulator of this invention, as schematically shown in Fig. 2, the second stage of the modulator comprises a first integrator 21 and a second integrator 22, a first loop coefficient switch 23, connected to the output of the first integrator 21 and switching between a first and a second loop coefficient e1 and e2 respectively, a second loop coefficient switch 24, constituting part of the feedback loop of the second stage and switching between a third and a fourth loop coefficient f1 and f1 respectively. The loop coefficients are connected to the second integrator 22. Further the modulator comprises a 1-bit/3-bit quantizer connected to the output of the second integrator 22, and a 1-bit/3-bit DAC 30 connected to the output of the quantizer 25 and constituting a first element of said feedback loop. The 1-bit/3-bit quantizer comprises a quantizer switch 26, a 1-bit quantizer 27, and a 3-bit quantizer 28, wherein said quantizer switch is arranged to switch between said 1-bit and 3-bit quantizers 28. The output of the 1-bit/3-bit quantizer 25 is further connected to a digital error correction logic 29, which provides an output to a decimator (not shown). The 1-bit/3-bit DAC comprises a 1-bit DAC 31, a 3-bit DAC 32, and a DAC-switch 33, arranged to switch between the outputs of said 1-bit and 3-bit DACs. The output of the DAC-switch 33 is connected to inter alia said second loop coefficient switch 24.

For those standards that have relatively low base-band widths, e.g. GSM with 100K Hz base-band, a high oversampling ratio can be easily achieved. In such cases the second stage's quantizer only needs 1-bit resolution

to meet the dynamic range specification, and thus the 1-bit quantizer 27 is switched in. Using a 1-bit quantizer eases the circuit design and saves both chip area and power. However in other standards like DECT, a much larger signal band reduces the achievable oversampling ratio severely due to the limitations of current design technology. With the example of DECT 700KHz base-band, an oversampling ratio of 32 means that OTAs have to operate under a sampling frequency of 44.8MHz, which is close to the state of the art of current OTA design. In such cases a multi-bit quantizer should be used in the second stage to further increase the dynamic range, and thus the 3-bit quantizer 28 is switched in. A mode selecting signal Φ is used to select a proper sampling frequency and a proper quantizer 27/28 for each standard mode. Thus, the mode selection signal Φ controls the first and second loop coefficient switches 23 and 24, the quantizer switch 26, and the DAC-switch 33. All the hardware components that have nothing to do with this switching mechanism are shared by all standards. The mode selection signal in turn is generated by another circuit of the multi-standard receiver, which circuit is able to identify the standard which the presently received radio signal complies with.

Figure 3 shows the switching method of 1-bit/3-bit quantizer 25 of the second stage. When operating in a specific standard mode, the proper quantizer is switched into use by the mode selection signal Φ. In accordance with a preferred embodiment of the present invention, when switching between 1-bit quantizer 27 and multi-bit quantizer 28, the power supply of unused quantizer is also switched off. Correspondingly, when switching between the 1-bit DAC 31 and the 3-bit DAC 32, the presently unused DAC is powered down. This eliminates unnecessary power consumption. The signal and power switches, i.e. the quantizer switch 26, can be realized

with properly sized transmission-gates, and more specifically by means of MOS transistors.

In switched capacitor circuit the loop coefficients are realized by the ratio between capacitors, which ideally is not related to their absolute values. However the kT/C noise consideration sets a minimum capacitor value in the high-resolution application. Also to be considered is the process mismatch, which limits the minimum value of the capacitors so that the deviation of capacitor ratio is under control. Within the limitation of the above two factors, the capacitor values should be selected as small as possible because the power used to charge and discharge these capacitors is directly proportional to their values. Since in different standard modes kT/C noise is of different level of importance, the minimum allowed capacitor values are also different. It is an embodiment of present invention to share part of the capacitors in all modes while switch in an extra amount of capacitor in each specific mode as needed, and thereby achieve the different loop coefficients e1, e2, f1 and f2 described above. This is illustrated in figure 4. Sampling capacitor Cs_1 and Integration capacitor Ci_1 are shared by all the operation modes. Upon necessity extra sampling capacitor Cs_2 and integration capacitor Ci_2 can be switched in. These extra capacitors have two effects on the circuit performance: 1) they can reduce the kT/C noise, and 2) they can also be used to change the integrator gain if $Cs\_2/Ci\_2 \neq Cs\_1/Ci\_1$. The later effect is useful because using a 1-bit quantizer or multi-bit quantizer will slightly change the optimized loop coefficients.

The OTAs in integrators are shared by all the standard modes. The OTAs are designed to meet the strictest specification of all the standards, yet still maintain small area and low power consumption. Thus they are designed to work under the highest sampling frequency with largest capacitance load that are required by all

the standards to be handled. These requirements can be translated into a set of specifications such as DC gain, bandwidth and slew-rate for OTA design. Basically the first and the last OTAs should have larger driving capability because their capacitance loads are relatively large. For the first OTA this large capacitance load comes from the kT/C noise considerations which leads to a large sampling and integration capacitor. For the last OTA this large capacitance load comes from the multi bit quantizer which includes an array of sample-hold circuits and comparators.

Above some examples of embodiments of the sigma-delta modulator of the present invention have been described. These examples should be considered non-limiting and many modifications will be evident to a man skilled in the art in the ligth of the description and within the scope of the invention as claimed. Below some examples of midifications will be addressed.

In Fig. 2 a 3-bit quantizer is disclosed. This is merely one example of a multi-bit quantizer, which is to be used according to the invention. Thus, other resolutions can be chosen as appropriate considering what different standards the modulator should be able to handle. Further, the resolution of the multi-bit DAC is adjusted accordingly.

CLAIMS

1. A sigma delta modulator, which is operative in different standard modes for processing communication signals of different communication standards, said modulator comprising a 1-bit quantizer and a multi-bit quantizer, and a switching mechanism for switching between said quantizers in dependence of the standard mode.

2. A sigma delta modulator according to claim 1, comprising a power control, which is arranged to power down the presently unused quantizer.

3. A sigma delta modulator according to claim 1 or 2, at least some loop coefficients of which are adjustable.

4. A sigma delta modulator according to claim 1, 2 or 3, comprising an integrator the gain of which is adjustable by adjustment of capacitor size.

5. A sigma delta modulator according to claim 4, wherein said adjustment of capacitor size is provided by a capacitor sharing mechanism comprising a plurality of capacitors, some of which are shared by all standard modes and some of which are selectively used in one or more specific modes.

6. A sigma delta modulator according to any one of the preceding claims, being of fourth order and comprising a cascade of two second order loops.

7. A sigma delta modulator according to claim 6, wherein said quantizers are comprised in the last loop.

8. An A/D converter comprising a sigma-delta modulator, which is operative in different standard modes for processing communication signals of different communication standards, said modulator comprising a 1-bit quantizer and a multi-bit quantizer, and a switching mechanism for switching between said quantizers in dependence of the standard mode.

9. An A/D converter according to claim 8, wherein said sigma delta modulator comprises an integrator the gain of which is adjustable by adjustment of capacitor size.

10. An A/D converter as claimed in claim 9, wherein said adjustment of capacitor size is provided by a capacitor sharing mechanism comprising a plurality of capacitors, some of which are shared by all standard modes and some of which are selectively used in one or more specific modes.

11. An A/D converter as claimed in claim 8, 9 or 10, comprising a power control for powering down presently unused parts of the A/D converter.

12. A multi-standard RF receiver comprising an A/D converter according to claim 8.

13. A method for signal processing of communication signals of different communication standards comprising the steps of determining what communication standard the communication signal belongs to, and sigma-delta modulating a base-band communication signal, which step comprises the step of, in dependence of the communication standard, either 1-bit quantizing or multi-bit quantizing the communication signal.

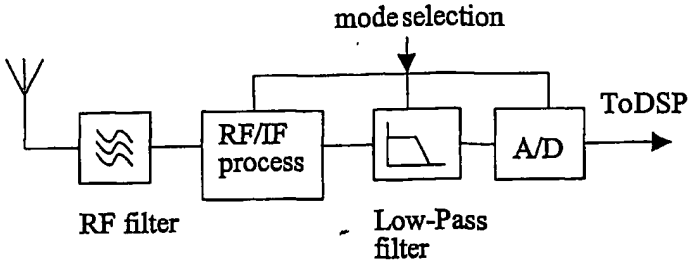
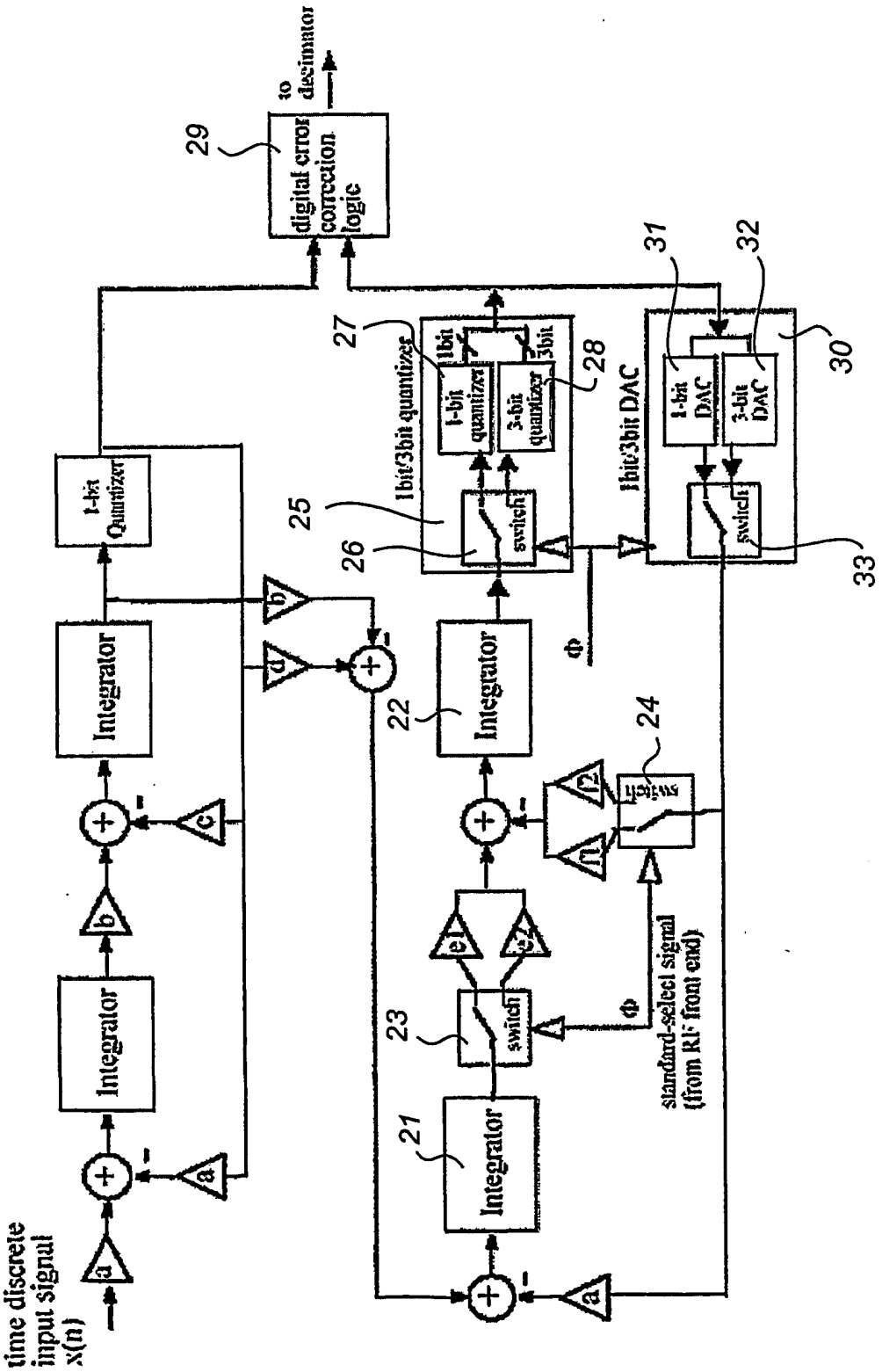


Fig. 1 A multi-standard receiver structure

Fig. 1

2/3


time discrete input signal x(n)
Integrator
Integrator
Integrator
Integrator
1-bit Quantizer
1bit/3bit quantizer
1-bit quantizer
3-bit quantizer
switch
switch
switch
1bit/3bit DAC
1-bit DAC
3-bit DAC
digital error correction logic
to decimator
standard-select signal (from RF front end)
21
22
23
24
25
26
27
28
29
30
31
32
33

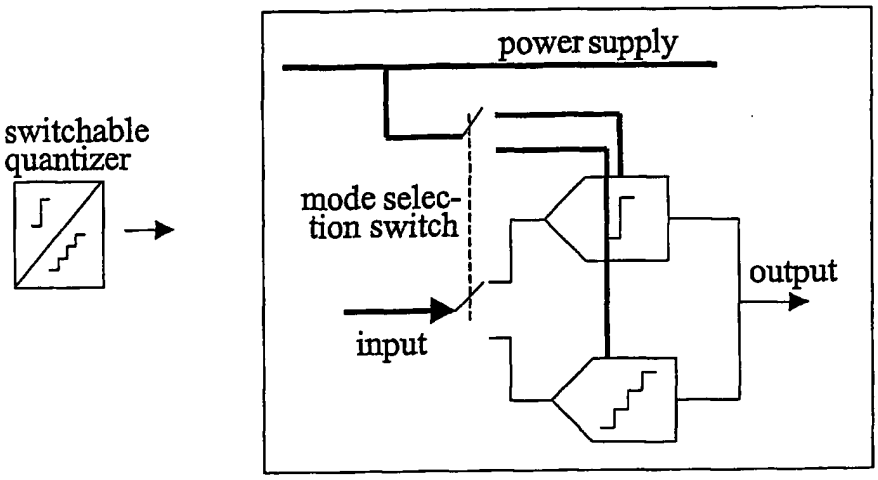

switchable
quantizer
power supply
mode selec-
tion switch
input
output

Fig. 3

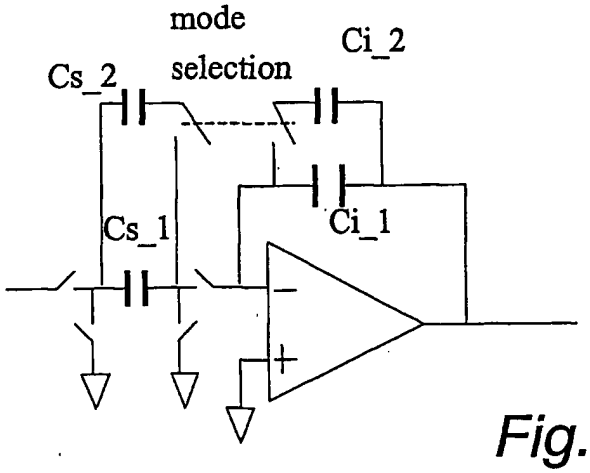

mode
selection
Cs_2
Ci_2
Cs_1
Ci_1

Fig. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 01/01214

A. CLASSIFICATION OF SUBJECT MATTER

IPC7: H03M 3/00, H03M 1/12
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7: H03M, H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-INTERNAL, WPI-DATA, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 9925075 A2 (KONINKLIJKE PHILIPS ELECTRONICS N.V.), 20 May 1999 (20.05.99), page 2, line 3 - page 3, line 25; page 5, line 4 - page 6, line 4; page 6, line 28 - page 7, line 13, page 8, line 4 - line 15	1,13
A	EP 0757446 A2 (NOKIA MOBILE PHONES LTD.), 5 February 1997 (05.02.97), column 2, line 45 - column 4, line 55	8-11
A	EP 0954107 A2 (MOTOROLA, INC.), 3 November 1999 (03.11.99), column 1, line 44 - column 2, line 11; column 2, line 35 - column 4, line 34	1-13

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 01/01214

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0454406 A1 (HUGHES AIRCRAFT COMPANY), 30 October 1991 (30.10.91), page 2, line 8 - line 19 ---	1-13
A	US 5345406 A (TIM A. WILLIAMS), 6 Sept 1994 (06.09.94), column 3, line 1 - line 50 --- ---	1-13

INTERNATIONAL SEARCH REPORT

Information on patent family members

02/08/01

International application No.
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		US 5153593 A	06/10/92
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